SMT HF SDR S/H (Sample and Hold) Receivers DR2G from 30 kHz to 70 (100) MHz - Make it Simple as Possible with Outstanding Performances

**Dipl. Ing . Tasić Siniša –Tasa YU1LM/QRP**

I started publishing my SDR series with wish to reject common opinion that isn't possible achieve and realize good performances without new, latest modern components. I also tried to enable new SDR technology for people from "third world ",easy and repeatable design to all without any RF experience and design for people which aren't SMT components lover. I also have a big collection classic size through holes components which ware reduced my design coast and enabled me endless experimenting. I have to admit that the new modern components have much better performances and designs are much more predictable than with old one. Professionally I am using SMT components but it is hard to design something new without appropriate PCBs. Experimenting with SMT resistors and capacitors are even much more simple and quickly that with classic size components when we have PCB.
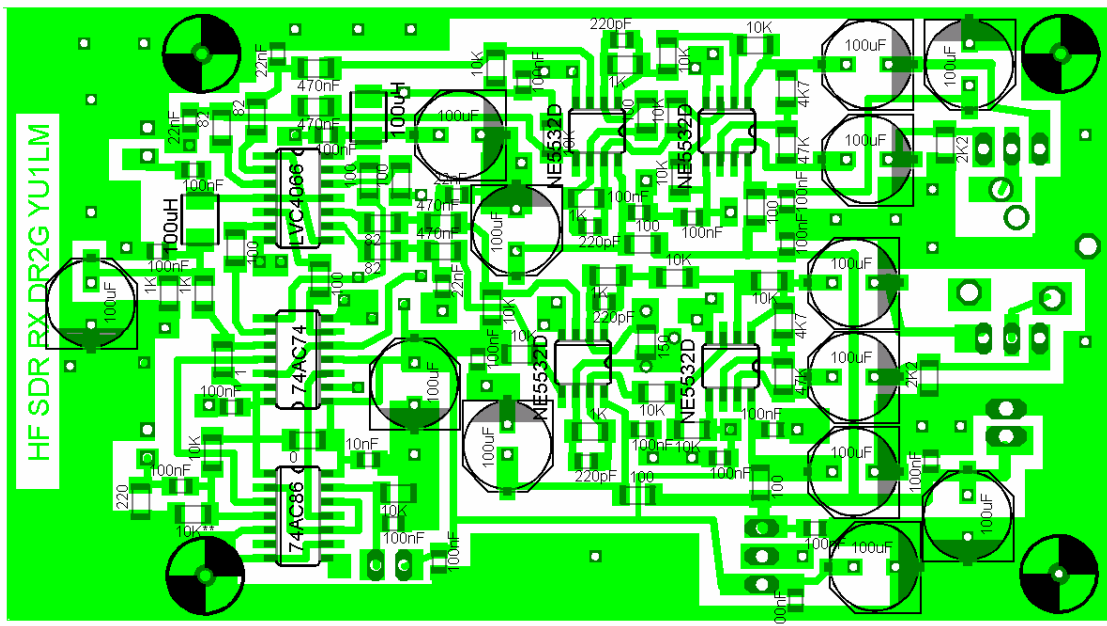
This new SDR DR2G receiver is my try to make simple as possible but very respectable performances SMT SDR receiver with two working modes optimal (4 times higher LO frequency) and non-optimal (LO twice higher). Optimal region is for lower frequencies to 50 MHz where we have need for much better RX performances demands that they are at higher frequencies. The double side PCB (one side back side is complete GND layer) was specially designed that it is possible their realization without metallization VIAs with few jumpers from back side only (see pictures inside text). This is also receiver which with new 74LVC*** series components can work to the 100 MHz without input band pass BP filters. I tried it to 75MHz because I couldn't find EXOR IC 74LVC86. I also enabled that we can use classic electrolytic capacitors instead SMT which is sometimes hard to find in adequate size.

DR2G design is compilation of different designs. It is based on previously published receivers DR2E, DR2A+ designs. The 74LVC4066 as main S/H elements has Rds-ON resistance in region 3-5 Ohms and their frequency limits is over 100 MHz range. IC FF 74AC74 is working to 140-145 MHz better substitute 74LVC74 works to 250MHz and EXOR 74AC86 to 140MHz 74LVC86 to 180-200 MHz.. These ICs are determining DR2G overall frequency limit performances. New better ICs enable much better performances and matching between switches in S/H detector circuit and because of that better hardware image rejection. Small Rds-ON is enabling better input IP3. Non optimal work in divide by 2 mode it isn't critical as it is with the old classic size components only it is important that input LO amplitude is high enough to enable correct dividing. Because of non optimal work good LO signal with close to the ideal sinusoidal shape or digital LO with 50/50 % ratio will enable good work in appropriate image rejection. It is important that is possible make fine adjustment image rejection with resistor 10K** to the GND at LO input close to the max LO frequency. If we adjust image rejection to the maximum, error from 90 deg at the beginning of non optimal frequency region will be acceptable. Of course it is possible adjust phase error in SDR software.
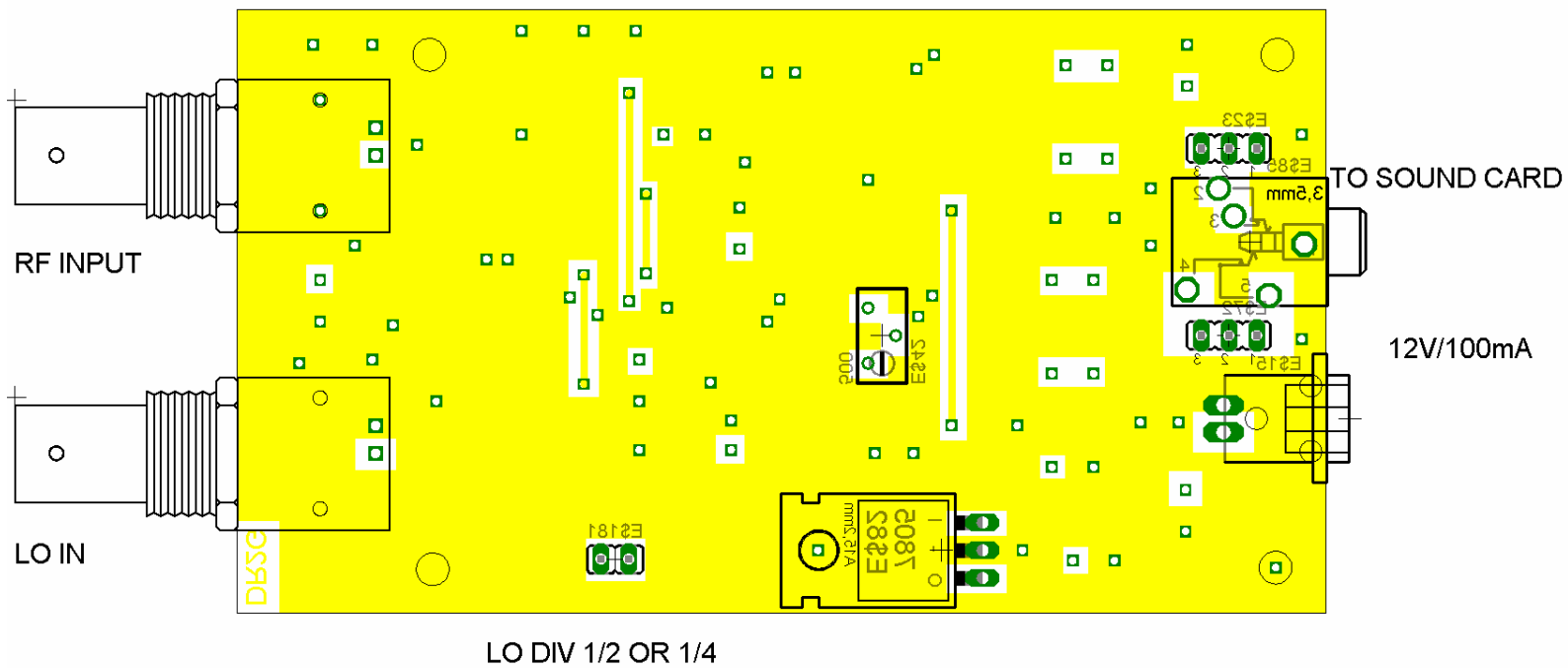
If we are using 74LVC74, for max input LO frequency, max power voltage supply have to be +3.3V. It is necessary to substitute 7805 with three terminal 3.3V voltage regulator IC.
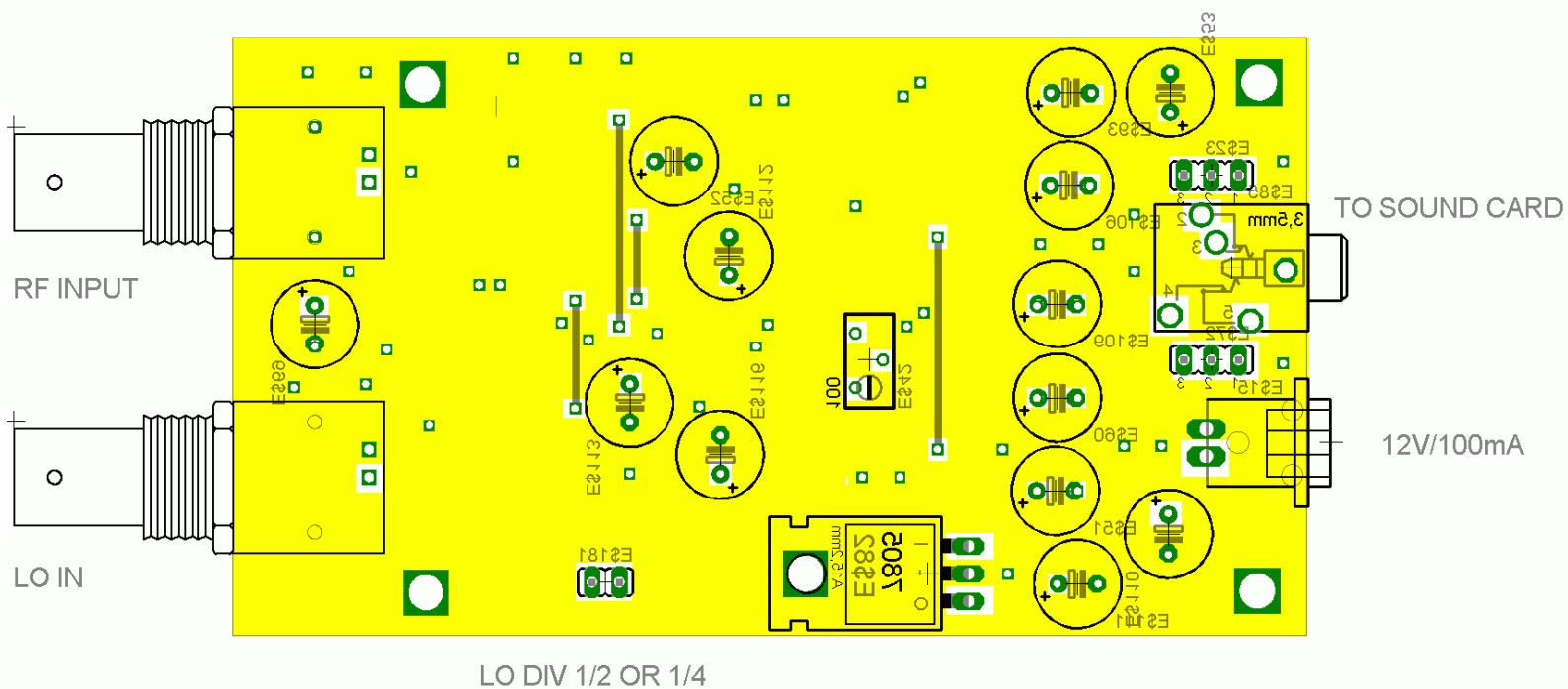
RF INPUT

LO IN

TO SOUND CARD

12V/100mA

LO DIV 1/2 OR 1/4
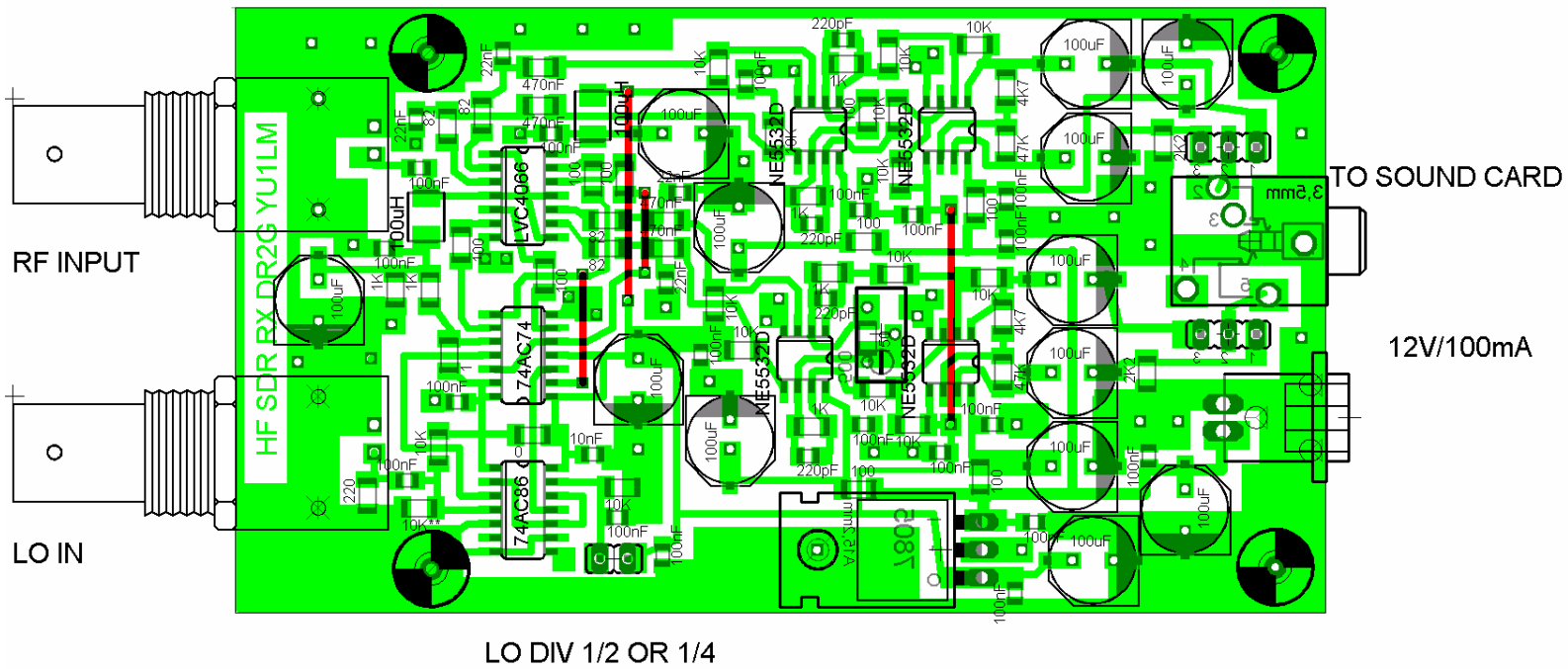
DR2G HF SDR SMT receiver double side PCB dimensions 55 x 100 mm(bottom side is GND layer)

DR2G top PCB elements placements

RF INPUT

LO IN

DR2G

E5181

300 E452

E582 7805

A15.2mm

TO SOUND CARD

3,5mm

E523

E585

E513

E515

12V/100mA

LO DIV 1/2 OR 1/4

DR2G bottom PCB parts placement

RF INPUT

LO IN

E5181

100 E452

E582 7805

A15.2mm

E593

E523

E585

E5106

E5109

E5113

E515

E512

E513

E519

E560

E561

E5110

E593

TO SOUND CARD

3,5mm

E513

E515

12V/100mA

LO DIV 1/2 OR 1/4
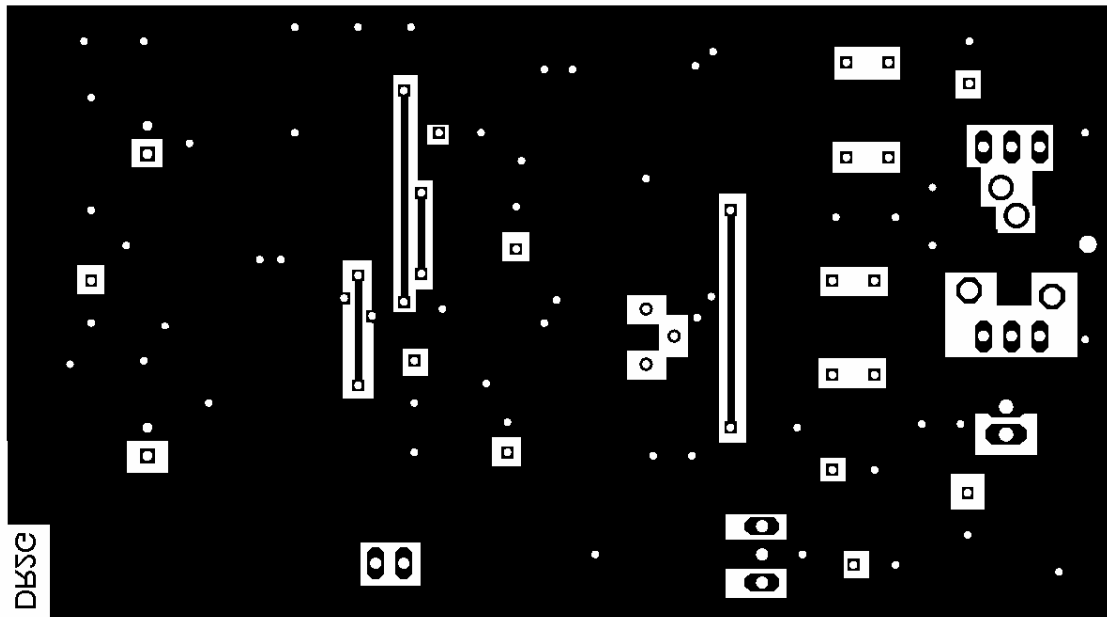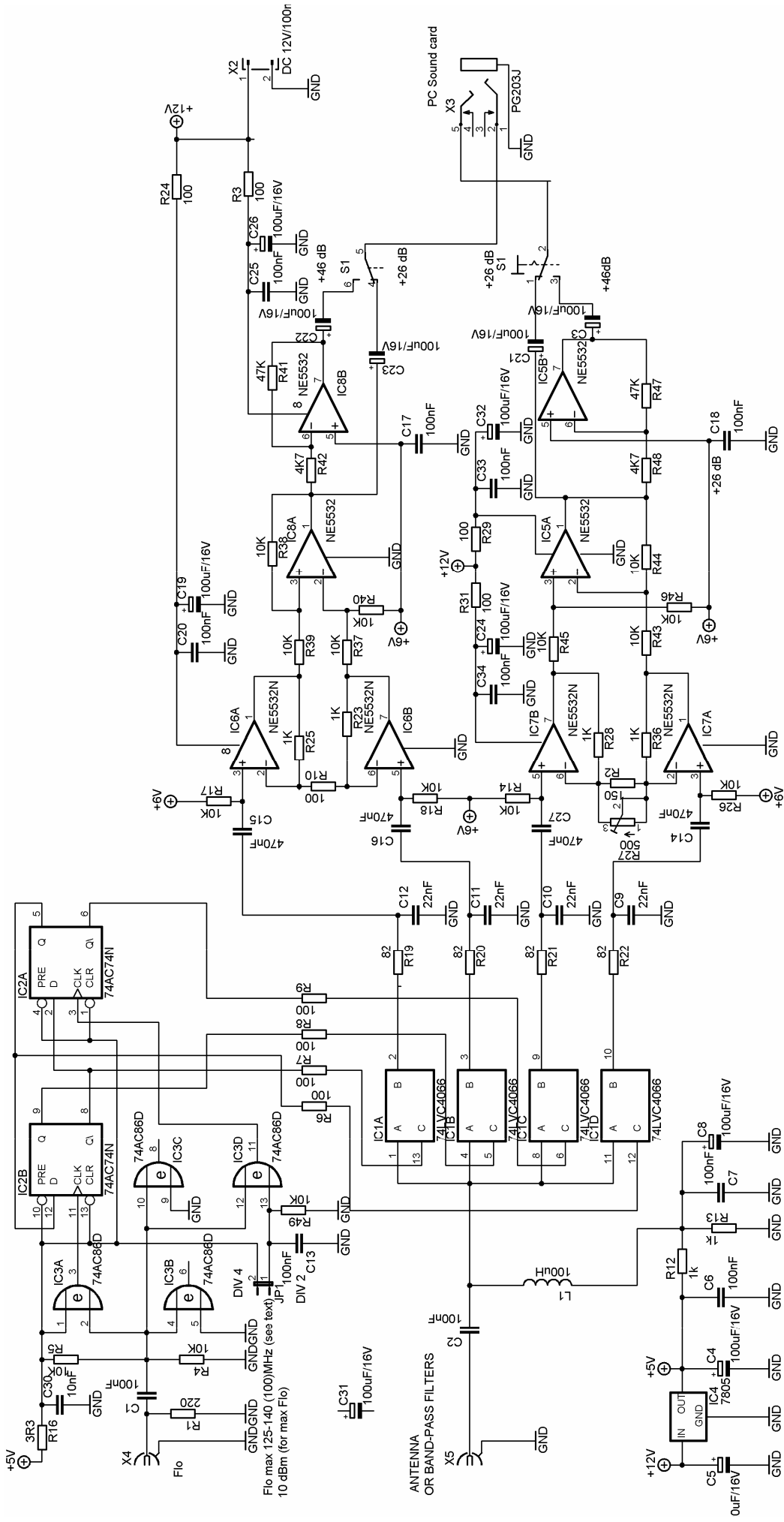
DR2G bottom PCB parts placement with classic through holes ELCO
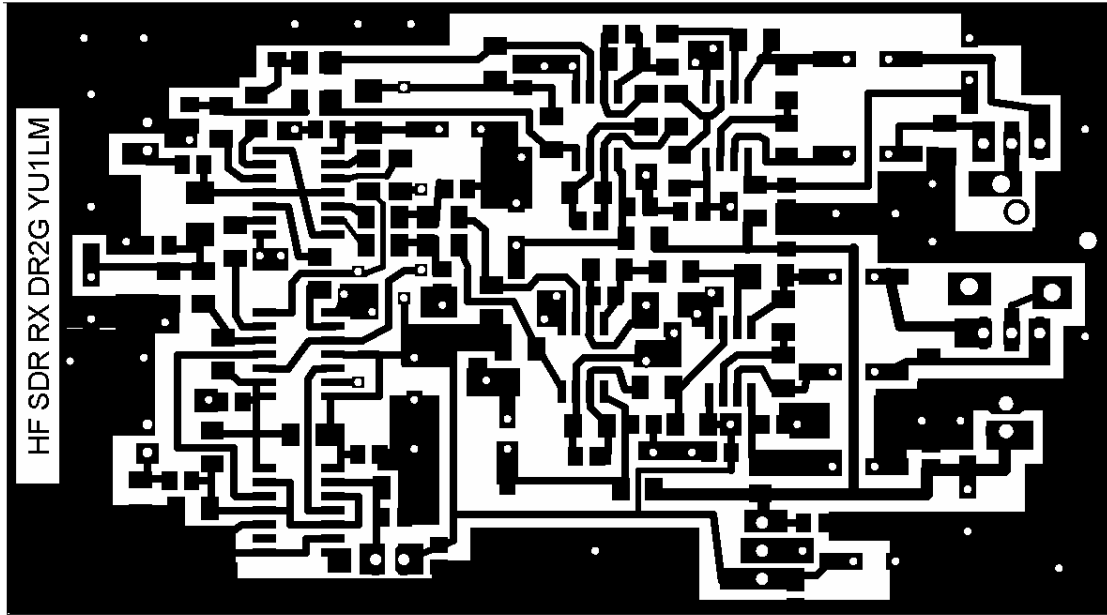
DR2G top PCB

DR2G bottom PCB

HF I/Q SDR Receiver DR2G
30 kHz-70(100) MHz   YU1LM/QRP

DR2G montage process if you haven't PCB with VIA-s

1.First it is necessary with borer diameters bigger then VIA's drill(1.5-2 mm) bottom copper surface to remove it at VIA's "hot" (not GND) points to prevent unwanted connections.
2.Next step is to solder wires at VIA places at both side and cut it close as possible at the top surface.
3. Then solder 4 wires from bottom size to enable correct connection (DR2G bottom PCB parts placement)
4. Next step is to solder SMT components from the top side
5.Last step is to solder components at bottom side

Example how VIAs and bottom side wires connection looks like

DR2G process adjustments are simple and done in two steps:

1.With 500OHms potentiometer adjust with DMM (digital multi meter) that resistance is 100 Ohms.
2.Second step is to with 500OHms potentiometer in SDR software adjust max image rejection best frequency is about 12-30 kHz from 0 Hz. This depend from SB sampling rate

Measuring results which I made with HF S/H SDR receiver DR2G

1.Receiving range is going from 30 kHz to 70(100) MHz.
2.IIP3 34-37dBm and it depends from setting and used programs.
3.MDS -120-122dBm also with 24 bit external USB SB card Audigy NX2
4.Image rejection is going from 35 -65 dB
5.DR2G sensitivity 0.3 - 0.6 uV for 10 dB S/N ratio, max S/N ratio I measured was 75 dB.
6.SFDR (Spurious free dynamic range) is 95-98 dB, this results are with signals spaced 5 kHz and more.

Some excellent performances aren't without other side:

1.First and very big disadvantage is 4 or 2 times higher LO
2.Image rejection is changing through receiving bands and results are done for frequencies 12 kHz from central frequency
.
    I wish you successful DR2G realization and I apologize for some possible mistakes. I made great effort to make SDR projects and share them with all who are interesting for. Anyway send me your comments positive or negative, results or photos of your realization please.

VY 73/72 and GL in SDR homebrew Tasa YU1LM/QRP

New E-mail address tasa@insimtel.com April 2007

stasic@eunet.yu

References:

1.   *www.qsl.net/yu1lm/homebrew*
2.   *http://forum.cqham.ru/viewforum.php ?f=28*
3.   *Skidan@mail.ints.net T03DSP UR3IQO http://users.ints.net/skidan/T03DSP*
4.   *http://www.nitehawk.com/sm5bsz Leif LINARD*
5.   *http://www.flex-radio.com SDR1000 Gerald AC5OG*
6.   *http://www.njqrp.org/mbrproj/9850dds.html*
www.analog.com/en/prod/0,,770_843_AD9850,00.html

http://www.qsl.net/pa3ckr/signalgenerator/

http://www.k6ese.com/DDS_Project.htm

http://ham.kiev.ua/pic/dds_ham2.html

http://www.qsl.net/om3cph/dds/rx.html

http://www.seboldt.net/k0jd/othervfo.html

http://perso.wanadoo.fr/f6itv/p2063001.htm

http://koti.netplaza.fi/~jonverro/ad9854.htm

http://www.labyrinth.net.au/~steve/freq/

http://members.aol.com/Dl4JAL/DDS.html

http://hem.passagen.se/communication/dds.html

7.   *Recent Advances in Shortwave Receiver Design Dr. Ulrich Rohde QST Nov 1992 page 53*
1.   *RF Design 6/1995*
2.   *Philips- Application note AN97090(IC gate overtone oscillator design)*

Software LINK for SDR radio receiving and transmitting

1.   *http://digilander.libero.it/i2phd/ SDRadio software ver 1.0*

   www.qsl.net/i2phd Alberto I2PHDhttp://gpsdo.i2phd.com/

2.   *ik2czl@weaksignals.com <ik2czl@weaksignals.com>ik2czl@weaksignals.com
<ik2czl@weaksignals.com>Vittorio*

3.   *www.weaksignals.com WINRAD*

4.   *www.ciaoradio.com*

5.   *www.m0kgk.co.uk/sdr*

6.   *www.g8jcf.dyndns.org Peter G8JCF*

7.   *http://www.nitehawk.com/sm5bsz Leif LINARD*
8.   *http://www.flex-radio.com SDR1000 Gerald AC5OG*
9.   *dl6iak.ba-karlsruhe.de*